

PACKAGING PROCESS FOR SEMICONDUCTOR PACKAGE

ABSTRACT

A packaging process for a semiconductor package is proposed, in which a plurality of conductive elements disposed on a substrate are electrically connected to the substrate and encapsulated by a first encapsulant formed on the substrate. Further, a semiconductor chip having a plurality of bond pads is mounted on a top surface of the first encapsulant and is electrically connected to the substrate through the bond pads being electrically connected to the corresponding conductive elements. Moreover, as the conductive elements have ends thereof coplanarly formed with the top surface of the first encapsulant, quality of the electrical connection between the chip and the conductive elements can be assured. In addition, as the conductive elements for electrically connecting the chip to the substrate are disposed on the substrate, the packaging cost can be reduced and quality of the packaged product can be improved. Finally, on two opposing surfaces of the substrate there are formed a second encapsulant for encapsulating the chip, and a plurality of solder balls, respectively, so as to complete the packaging of the invention.

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